Application Note

How to Program SPI NOR Flash and EEPROM on StarProg-A

Version 1.1

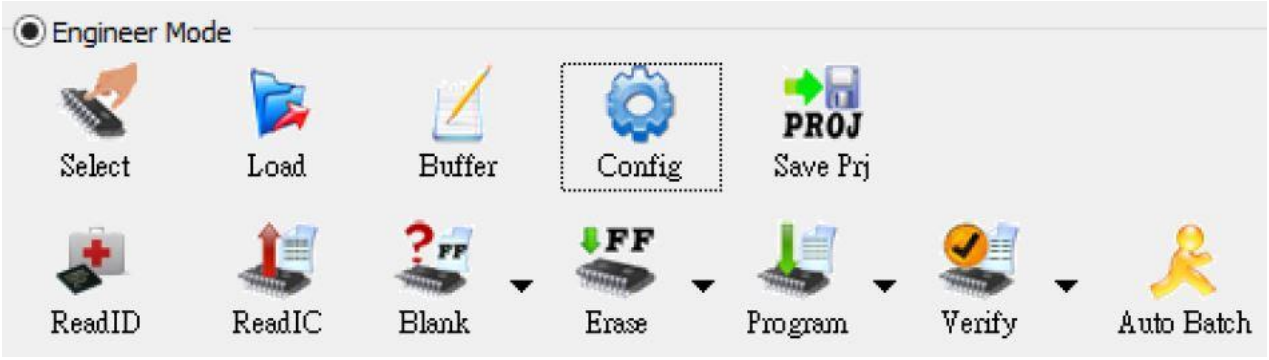
DediProg

Table of Content:

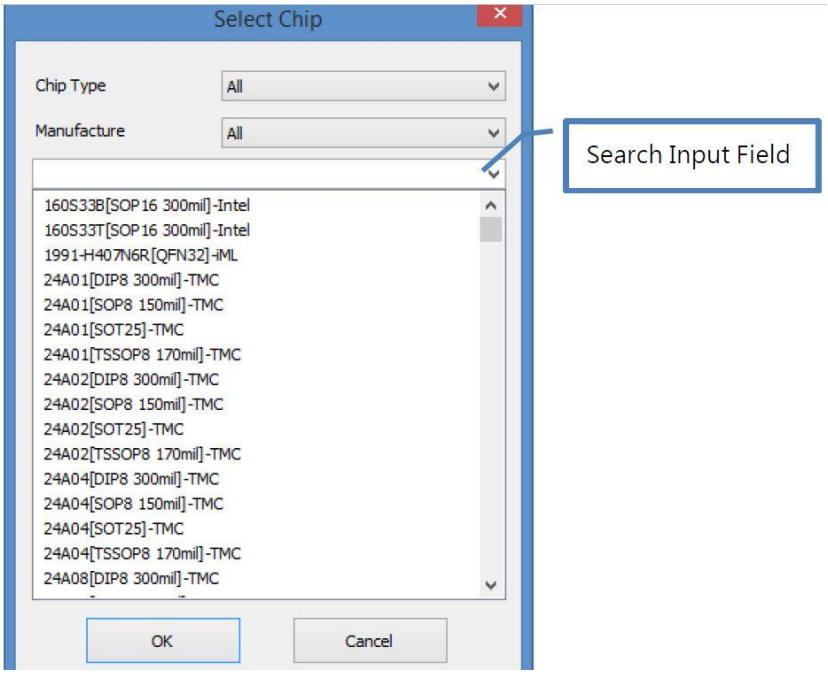
I. Description

This application note illustrates how to program EEPROM and SPI NOR Flash with Dual die on StarProg-A, including EEPROM 24,25,93,95 series, Micron MT25TL series, Macronix MX66L1G85G、MX66L51285G and Spansion S79FL series. Learn more about DediProg products and how to use them.

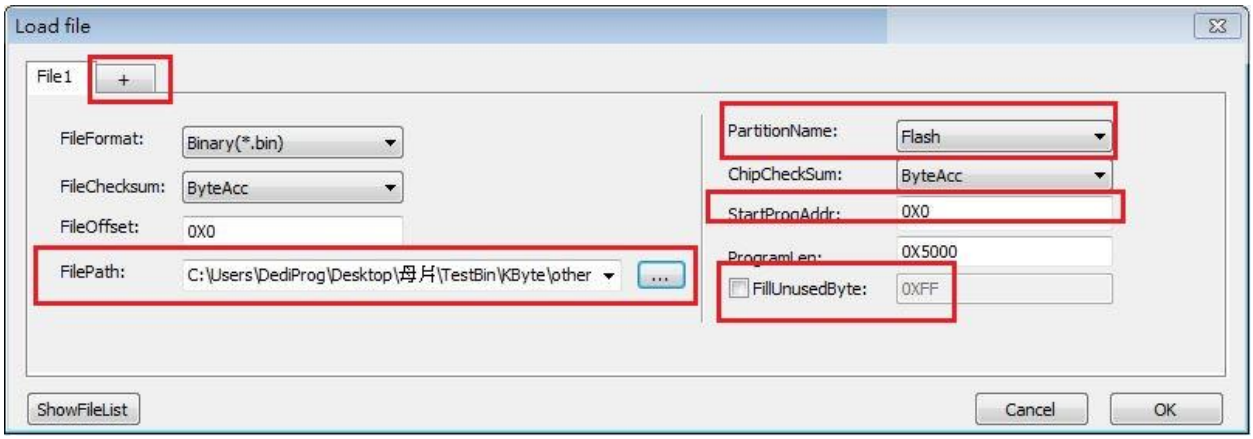
II. Dediware Procedure



2.1 Select: Click “Select” to choose IC manufacturer/part number/package 

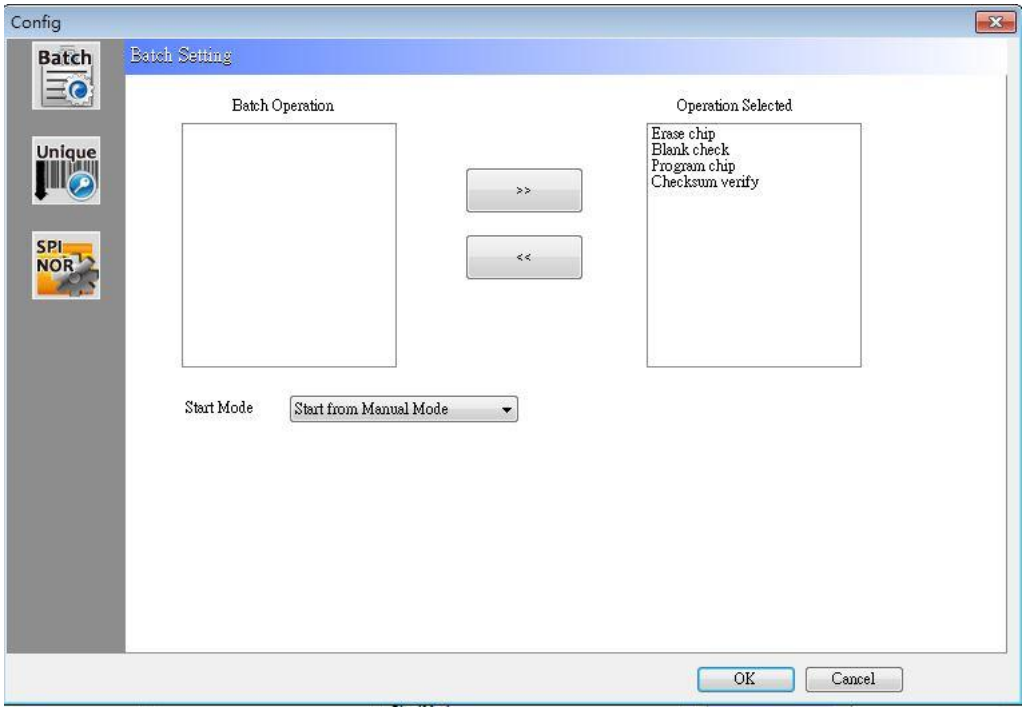


2.2 Load: Click “Load” to load the file intended for the programmer 



+: Add other partition to load file
FilePath: Show your file path
PartitionName: Indicate the partition that you request
StartProgAddr: Indicate the start address
FillUnusedByte: Select to fill unused byte, ex: 0xFF

2.3 Config: Set up batch operation and options 



2.4 Programming function

2.4.1 Read ID: If IC has readable ID that can show in the Log window, then the ID will appear in the ChipInfo.

2.4.2 Read IC: Read the IC data and compare with the file data.

2.4.3 Erase: Erase entire IC or specific area if IC has several partitions.

2.4.4 Blank Check: Check if the target chip is blank or not.

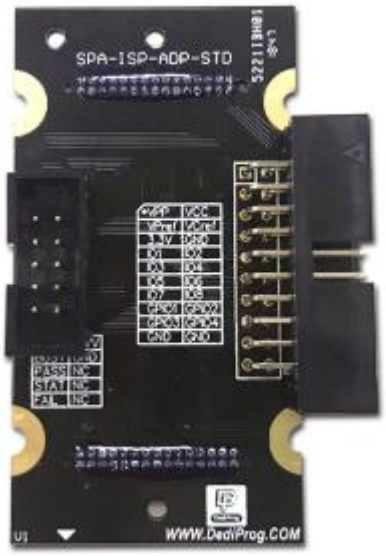
2.4.5 Program: Write the selected file data into the chip.

2.4.6 Verify: Content verification between chips and loaded file.

2.4.7 Auto Batch: Run the programming settings of batch in Config.

III. ISP Adaptor (SPA-ISP-ADP-STD) Pin Out

SPA-ISP-ADP-STD



ISP Adaptor ICP Port

Pin header mapping			
Pin lin1	Pin number		Pin lin2
Vpp	1	2	Vcc
Vpp_ref	3	4	Vcc_ref
3.3V	5	6	GND
IO1	7	8	IO2
IO3	9	10	IO4
IO5	11	12	IO6
IO7	13	14	IO8
GPIO1	15	16	GPIO2
GPIO3	17	18	GPIO4
GND	19	20	GND

ISP Adaptor ATE Port

ATE			
Pin lin1	Pin number		Pin lin2
NC	1	2	3.3V
Busy	3	4	GND
Pass	5	6	NC
Start	7	8	NC
Fail	9	10	NC

IV. EEPROM

- **EEPROM 24 Series**

	IC	SPA-ISP-ADP-STD
Pin assignment	A0(Pin1)	IO1
	A1(Pin2)	IO2
	A2(Pin3)	IO3
	GND(Pin4)	GND
	SDA(Pin5)	IO5
	SCL(Pin6)	IO6
	WP(Pin7)	IO7
	VCC(Pin8)	VCC

Note:

1. SCL, SDA need to pull up (3.3K~10K ohm) to VCC.
2. If programming is unstable, VCC can connect a cap. (4.7uF) to GND.

- **EEPROM 25 Series**

	IC	SPA-ISP-ADP-STD
Pin assignment	CS(Pin1)	IO1
	MISO(Pin2)	IO2
	WP(Pin3)	VPP
	GND(Pin4)	GND
	MOSI(Pin5)	IO5
	CLK(Pin6)	IO6
	HOLD(Pin7)	IO7
	VCC(Pin8)	VCC

Note:

1. If programming is unstable, CLK can connect a cap. (33pF) to GND.
2. If programming is unstable, VCC can connect a cap. (4.7uF) to GND.

- **EEPROM 93 Series**

	IC	SPA-ISP-ADP-STD
Pin assignment	CS(Pin1)	IO1
	SK(Pin2)	IO2
	DI(Pin3)	VPP
	DO(Pin4)	IO4
	GND(Pin5)	GND
	ORG(Pin6)	IO6
	NC(Pin7)	IO7
	VCC(Pin8)	VCC

Note:

3. If programming is unstable, CLK can connect a cap. (33pF) to GND.
1. If programming is unstable, VCC can connect a cap. (4.7uF) to GND.

- **EEPROM 95 Series**

	IC	SPA-ISP-ADP-STD
Pin assignment	S(Pin1)	IO1
	Q(Pin2)	IO2
	W(Pin3)	VPP
	VSS(Pin4)	GND
	D(Pin5)	IO5
	C(Pin6)	IO6
	HOLD(Pin7)	IO7
	VCC(Pin8)	VCC

Note:

1. If programming is unstable, CLK can connect a cap. (33pF) to GND.
2. If programming is unstable, VCC can connect a cap. (4.7uF) to GND.

V. SPI

	IC	SPA-IPS-ADP-STD
Pin assignment	CS(Pin1)	IO1
	MISO(Pin2)	IO2
	WP(Pin3)	IO3
	GND(Pin4)	GND
	MOSI(Pin5)	IO5
	CLK(Pin6)	IO6
	HOLD(Pin7)	IO7
	VCC(Pin8)	VCC

Note:

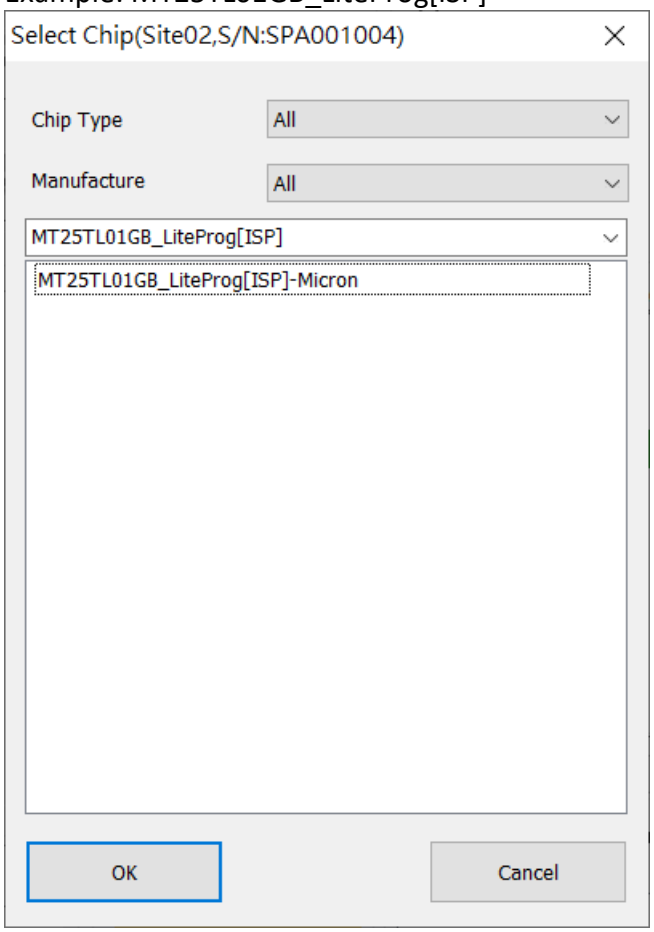
2. If programming is unstable, CLK can connect a cap. (33pF) to GND.
3. If programming is unstable, VCC can connect a cap. (4.7uF) to GND.

VI. Dual Die

6.1 Micron MT25TL 25 Series

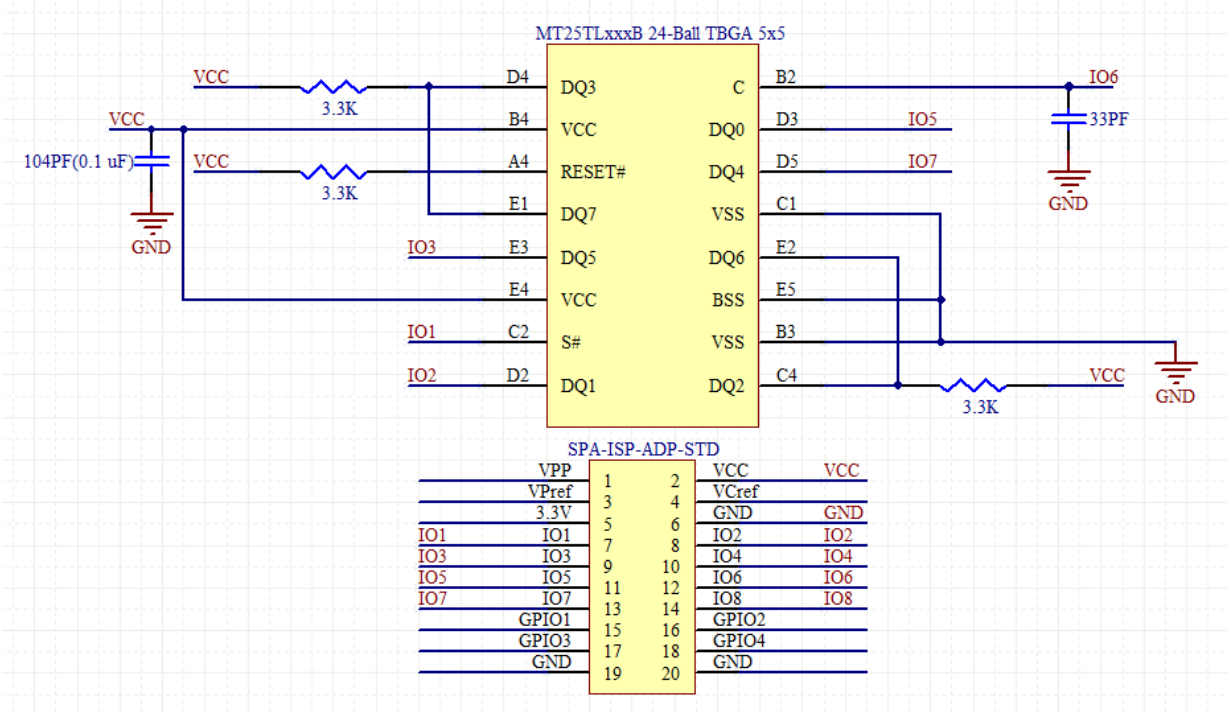
Please select the Part Number with the underline **"_LiteProg"**

Example: MT25TL01GB_LiteProg[ISP]

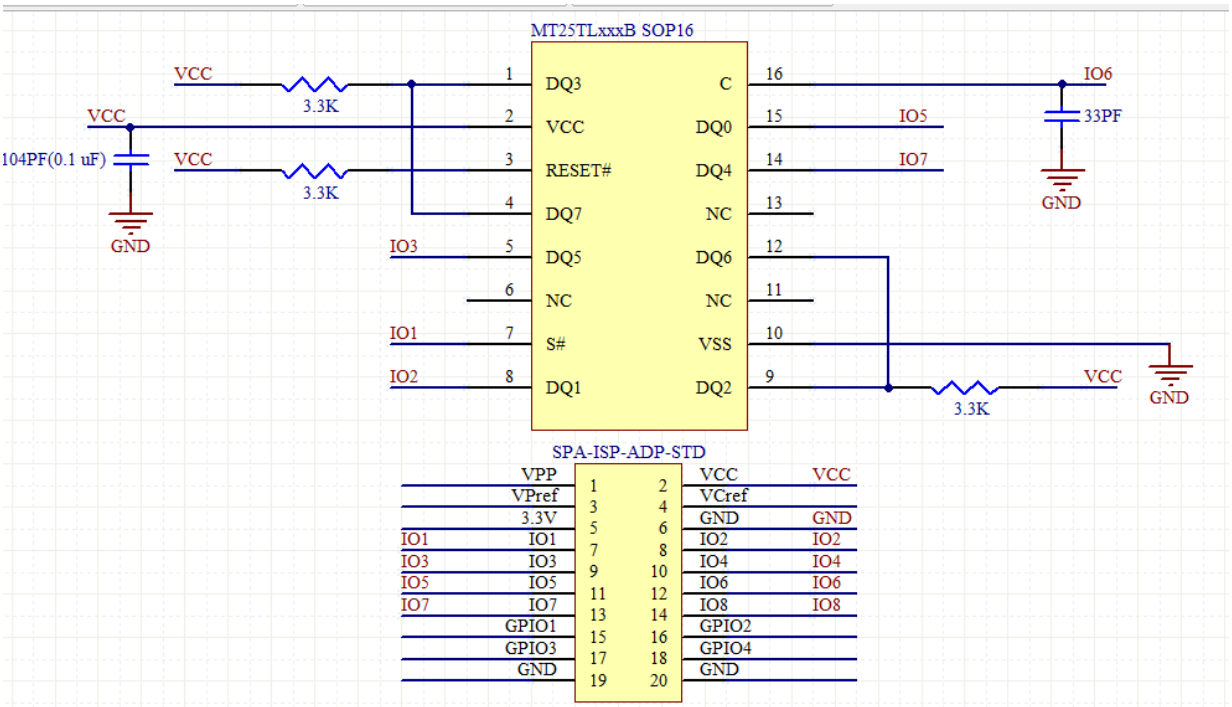


6.1.1 Application circuit

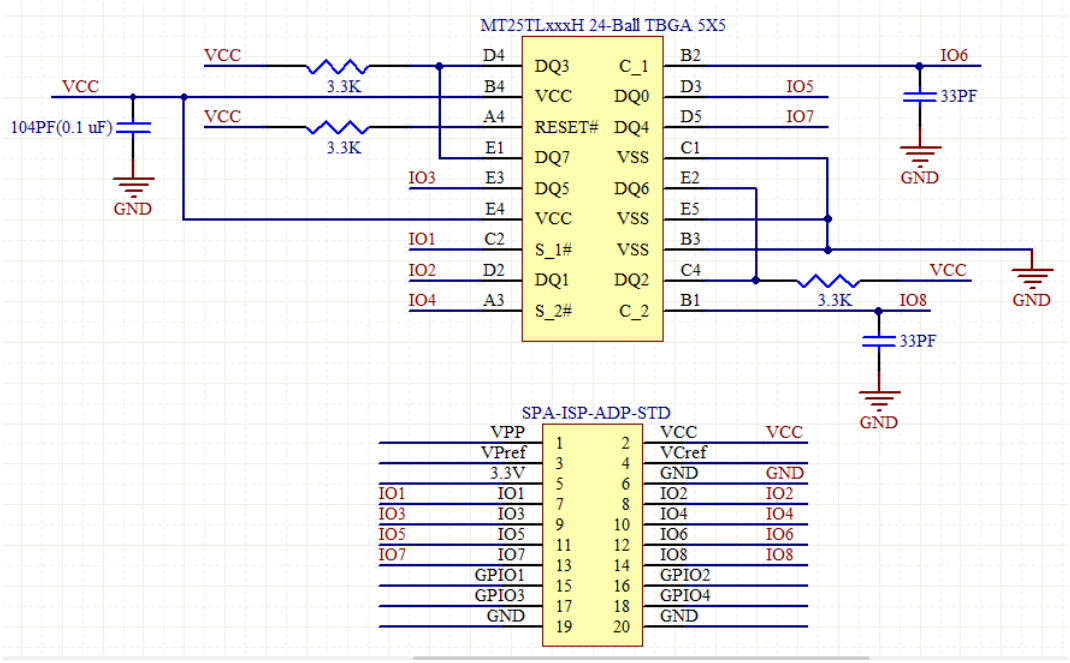
- MT25TLxxxB 24-Ball TBGA – 5 x 5



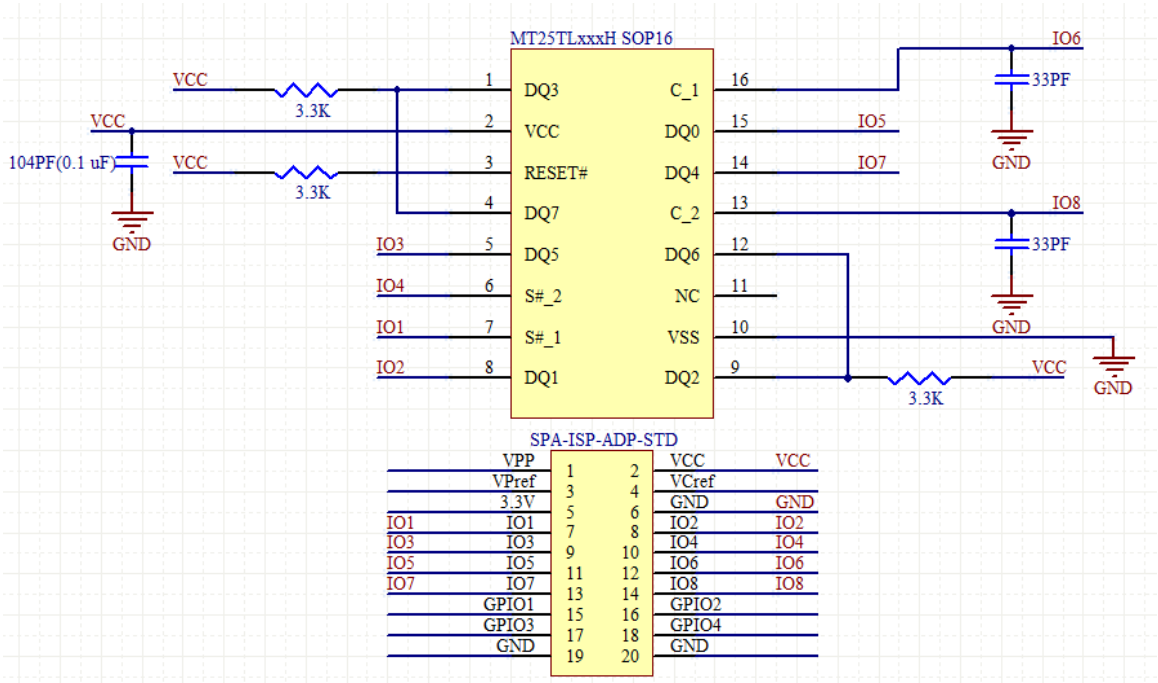
- MT25TLxxxB SOP16



- MT25TLxxxH 24-Ball TBGA – 5 x 5



- MT25TLxxxH SOP16



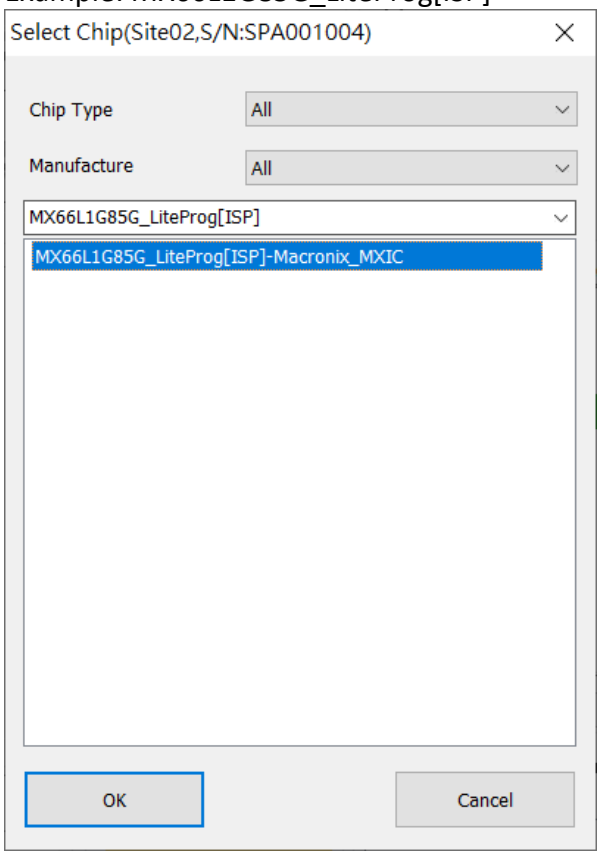
6.1.2 Partition define in Dediware

- **Partition 1：NOR die 1 Memory**
- **Partition 2：NOR die 2 Memory**
- **Partition 3：NOR die 1 64 OTP bytes**
- **Partition 4：NOR die 2 64 OTP bytes**
- **Partition 5：Config**

6.2 Macronix MX66L1G85G/MX66L51285G

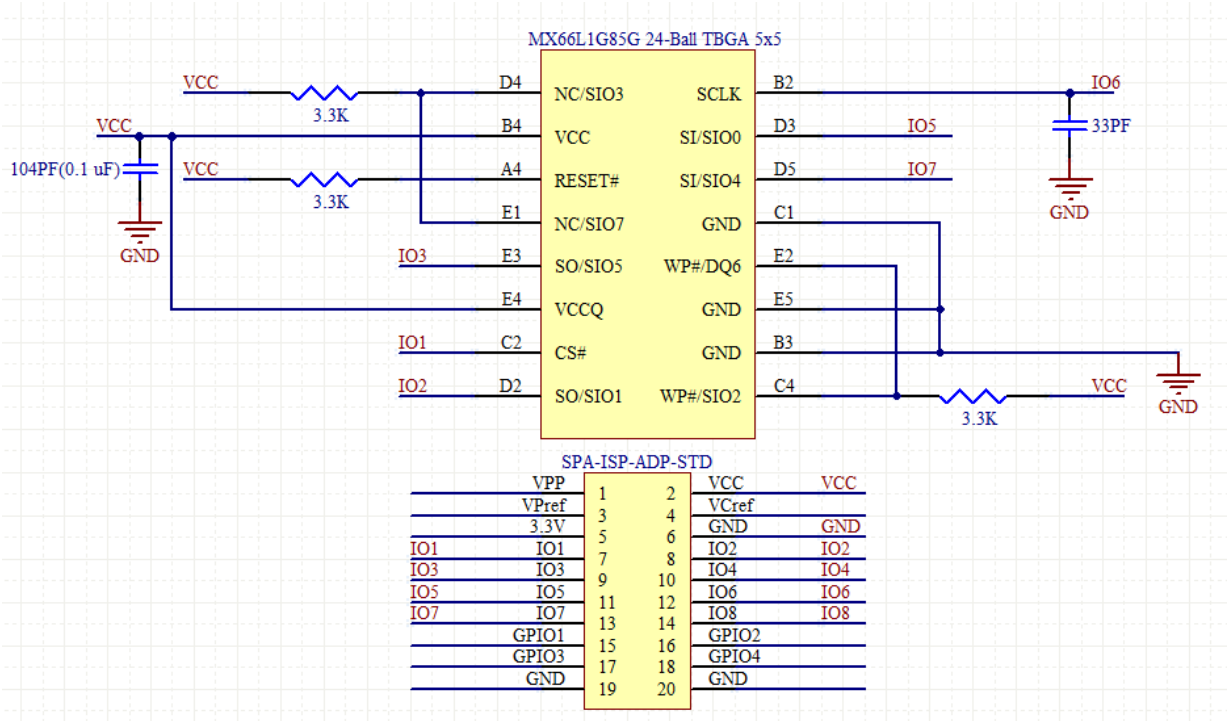
Please select the Part Number with the underline **"_LiteProg"**

Example: MX66L1G85G_LiteProg[ISP]

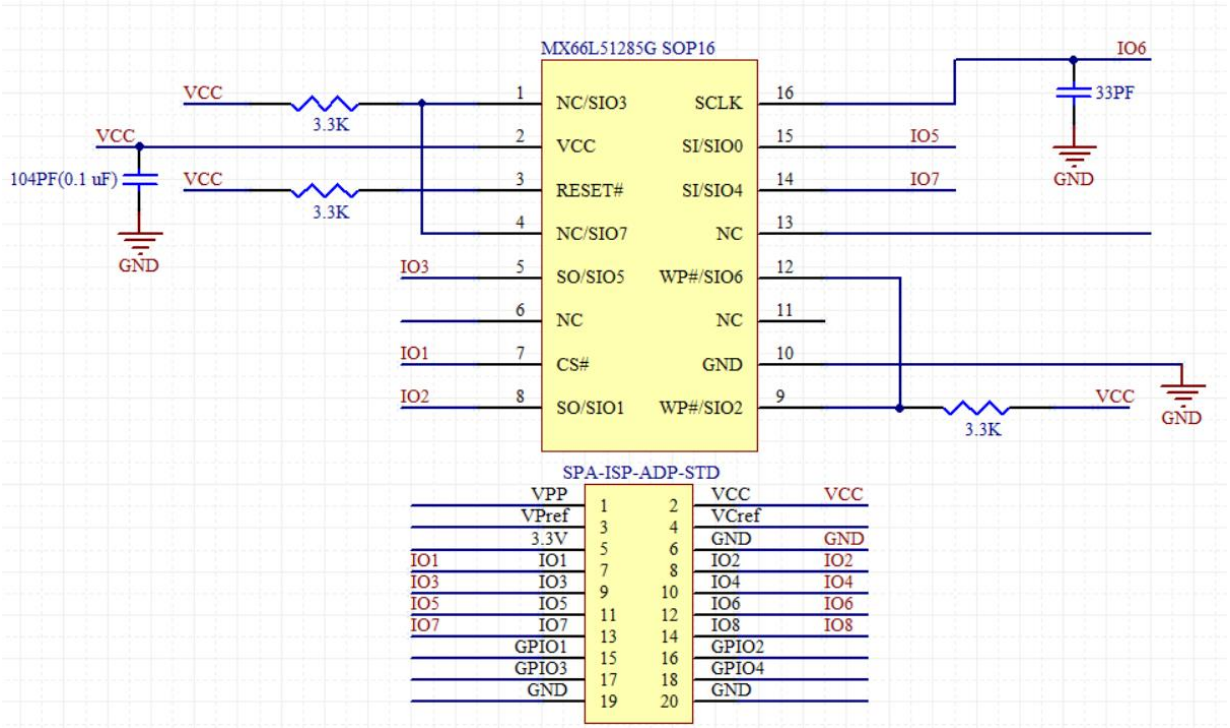


6.2.1 Application Circuit

- MX66L1G85G/MX66L51285G 24-Ball TBGA – 5 x 5



- MX66L51285G/MX66L25685G SOP16



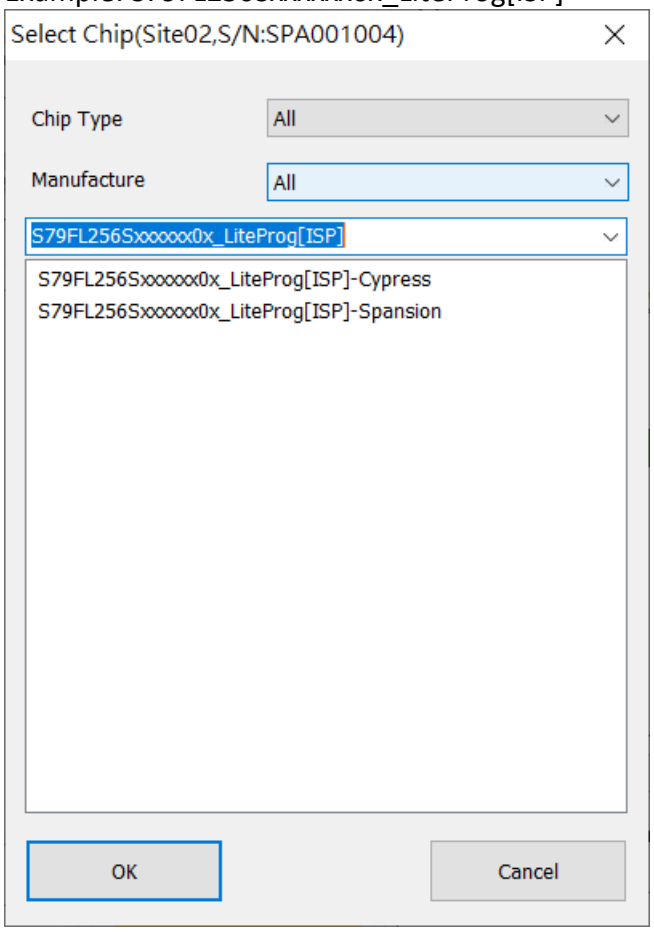
6.2.2 Partition define in Dediware

- **Partition 1：NOR die 1 Memory**
- **Partition 2：NOR die 2 Memory**
- **Partition 3：NOR die 1 4K-bit secured OTP**
- **Partition 4：NOR die 2 4K-bit secured OTP**
- **Partition 5：Config**

6.3 Spansion S79FL / Cypress S98FL Series

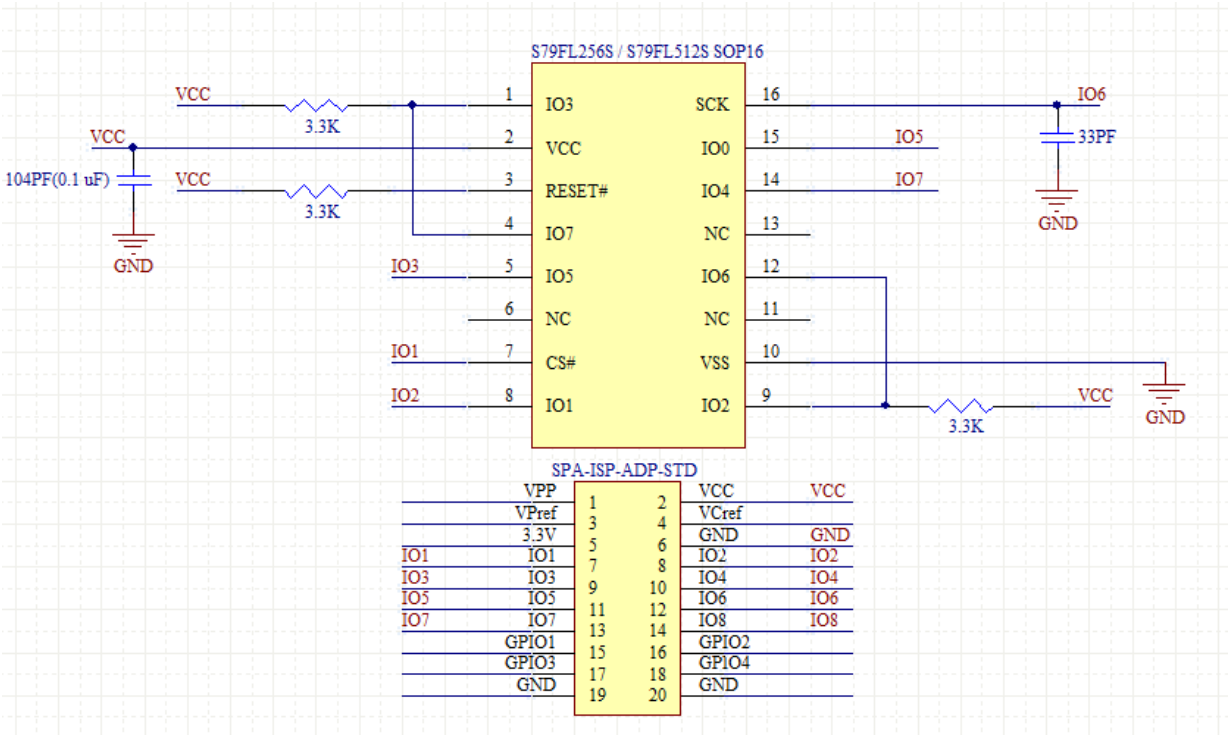
Please select the Part Number with the underline **"_LiteProg"**

Example: S79FL256Sxxxxxx0x_LiteProg[ISP]

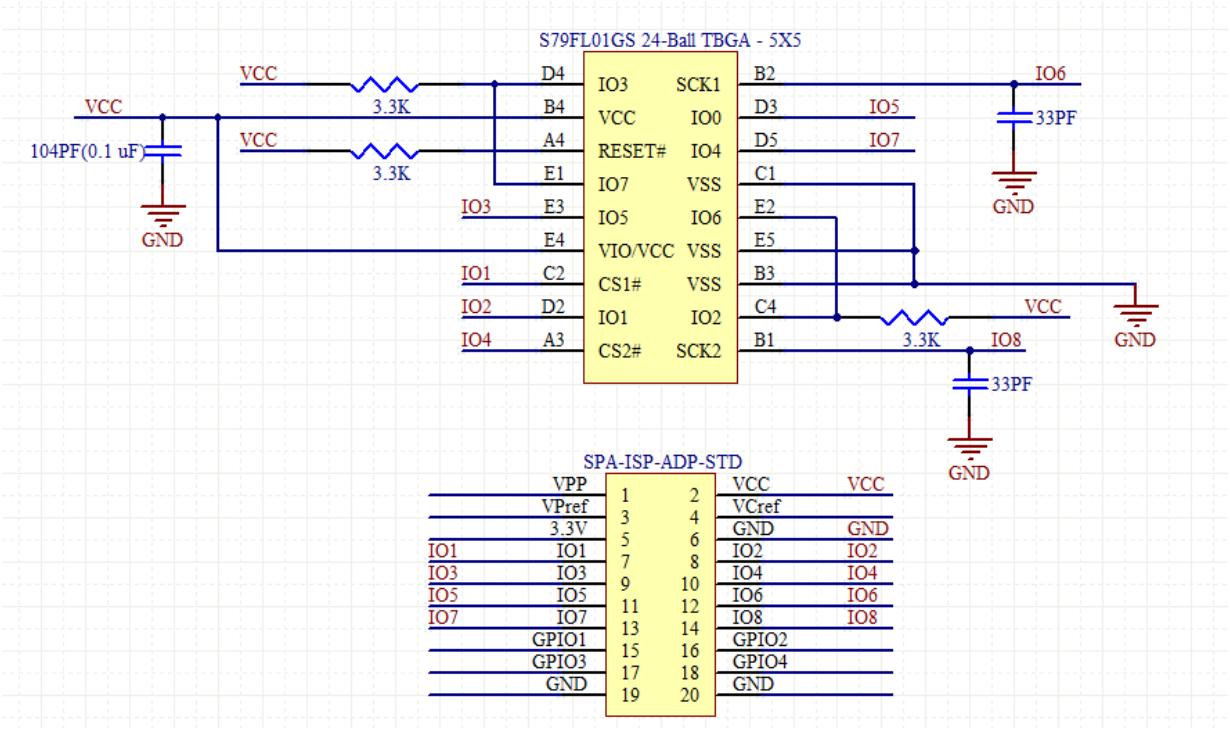


6.3.1 Application Circuit

- S79FL256S / S79FL512S / S98FL256S / S98FL512S



- S79FL01GS / S98FL01GS



6.3.2 Partition define in Dediware

- Partition 1：NOR die 1 Memory
- Partition 2：NOR die 2 Memory
- Partition 3：NOR die 1 2048 bytes OTP
  - S79FL256S / S98FL256S

    Buffer configuration of OTP memory：

Region 0			
OTP Address	0h-Fh	10h-13h	14h-1Fh
Buffer Address		2000000h-2000003h	2000004h-200000Fh
Name of area	Spansion Programmed Random Number	OTP Lock Bytes	Reserved for Future Use (RFU)

Region 1-31			
OTP Address	20h-3Fh	…..	7E0h-7FFh
Buffer Address	2000010h-200002Fh	…..	20007D0h-20007Efh
Name of area	Region 1	…..	Region 31

  - S79FL512S / S98FL512S

		Region 0	
OTP Address	0h-Fh	10h-13h	14h-1Fh
Buffer Address		4000000h-4000003h	4000004h-400000Fh
Name of area	Spansion Programmed Random Number	OTP Lock Bytes	Reserved for Future Use (RFU)

Region 1-31			
OTP Address	20h-3Fh	…..	7E0h-7FFh
Buffer Address	4000010h-400002Fh	…..	40007D0h-40007Efh
Name of area	Region 1	…..	Region 31

  - S79FL01GS / S98FL01GS

		Region 0	
OTP Address	0h-Fh	10h-13h	14h-1Fh
Buffer Address		8000000h-8000003h	8000004h-800000Fh
Name of area	Spansion Programmed Random Number	OTP Lock Bytes	Reserved for Future Use (RFU)

Region 1-31			
OTP Address	20h-3Fh	…..	7E0h-7FFh
Buffer Address	8000010h-800002Fh	…..	80007D0h-80007Efh
Name of area	Region 1	…..	Region 31

- Partition 4：NOR die 2 2048 bytes OTP
  - S79FL256S / S98FL256S

Buffer configuration of OTP memory：

Region 0			
OTP Address	0h-Fh	10h-13h	14h-1Fh
Buffer Address		3000000h-3000003h	3000004h-300000Fh
Name of area	Spansion Programmed Random Number	OTP Lock Bytes	Reserved for Future Use (RFU)

Region 1-31			
OTP Address	20h-3Fh	…..	7E0h-7FFh
Buffer Address	3000010h-300002Fh	…..	30007D0h-30007Efh
Name of area	Region 1	…..	Region 31

  - S79FL512S / S98FL512S

• Region 0			
OTP Address	0h-Fh	10h-13h	14h-1Fh
Buffer Address		5000000h-5000003h	5000004h-500000Fh
Name of area	Spansion Programmed Random Number	OTP Lock Bytes	Reserved for Future Use (RFU)

Region 1-31			
OTP Address	20h-3Fh	…..	7E0h-7FFh
Buffer Address	5000010h-500002Fh	…..	50007D0h-50007Efh

  - S79FL01GS / S98FL01GS

• Region 0			
OTP Address	0h-Fh	10h-13h	14h-1Fh
Buffer Address		9000000h-9000003h	9000004h-900000Fh
Name of area	Spansion Programmed Random Number	OTP Lock Bytes	Reserved for Future Use (RFU)

Region 1-31			
OTP Address	20h-3Fh	…..	7E0h-7FFh
Buffer Address	9000010h-900002Fh	…..	90007D0h-90007Efh
Name of area	Region 1	…..	Region 31

- Partition 5：Config

VII. Revision History

Date	Version	Changes
2019/06/21	1.0	Initial release
2021/07/12	1.1	Add MX66L25685G Pin Out

DediProg Technology Co., Ltd.

Taiwan Headquarter TEL: 886-2-2790-7932 FAX: 886-2-2790-7916
4F., No.7, Ln. 143, Xinming Rd., Neihu Dist., Taipei City 114, Taiwan

China Office TEL: 86-21-5160-0157
Room 518, Building 66, Lane1333, Xinlong Road, Vanke Hongqiao CBD.Min Hang District, Shanghai, P.R.C. 201101

U. S. Office TEL: 1-909-274-8860
209 E Baseline RD, Suite E208 #8, Tempe, AZ, 85283, USA

Technical Support: **support@dediprog.com** Sales Support: **sales@dediprog.com**